Fig.1 (Prior Art)

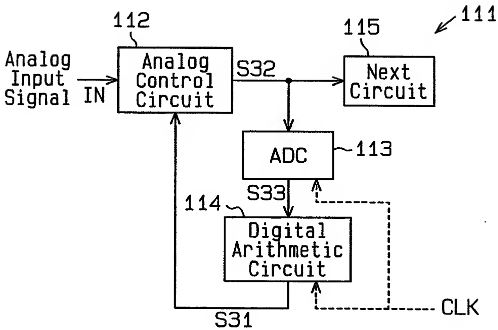


Fig.2 (Prior Art)

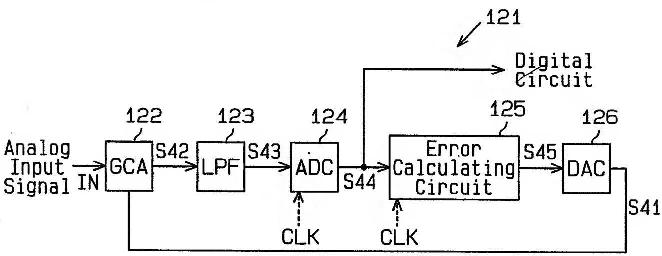


Fig.3(Prior Art)

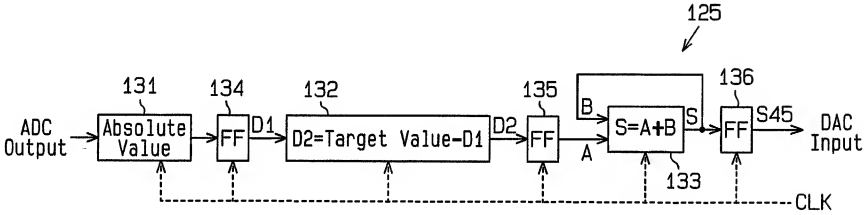


Fig.4(Prior Art)

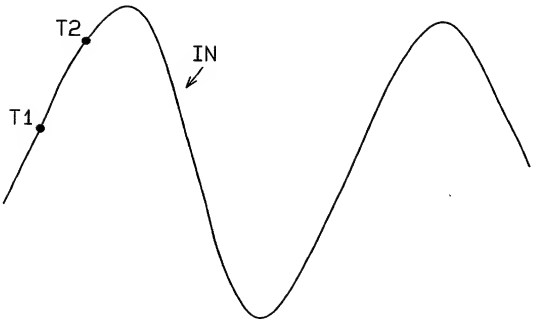


Fig.5

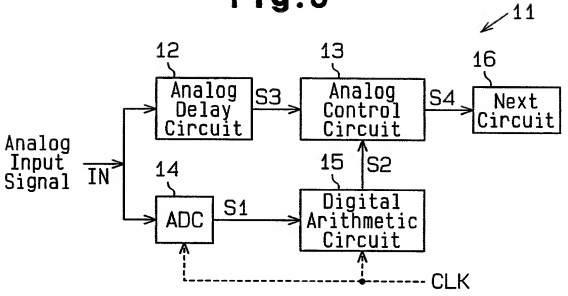


Fig.6

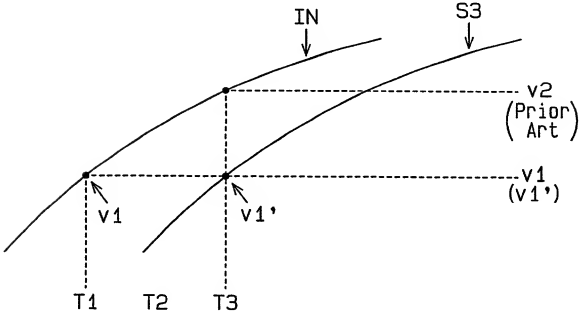


Fig.7

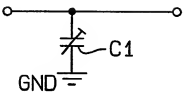


Fig.8

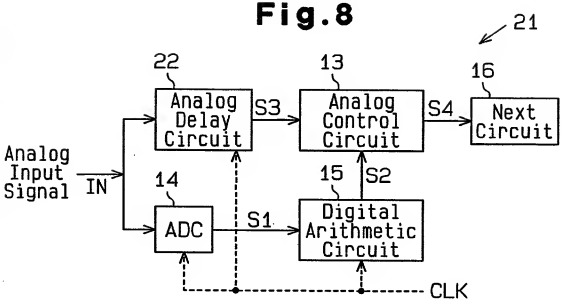


Fig.9

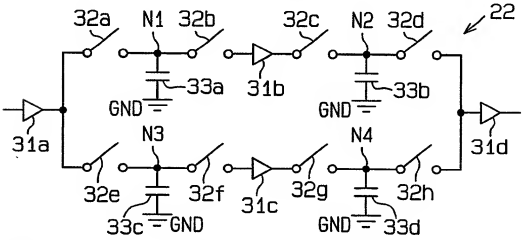


Fig.10

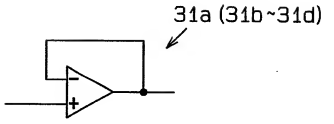


Fig.11

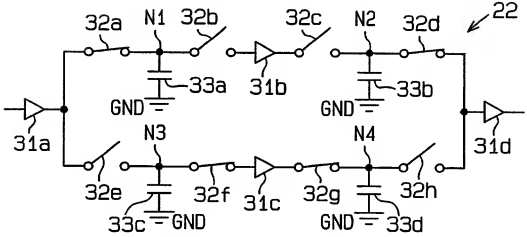


Fig.12

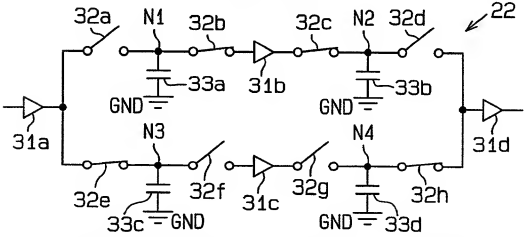


Fig.13

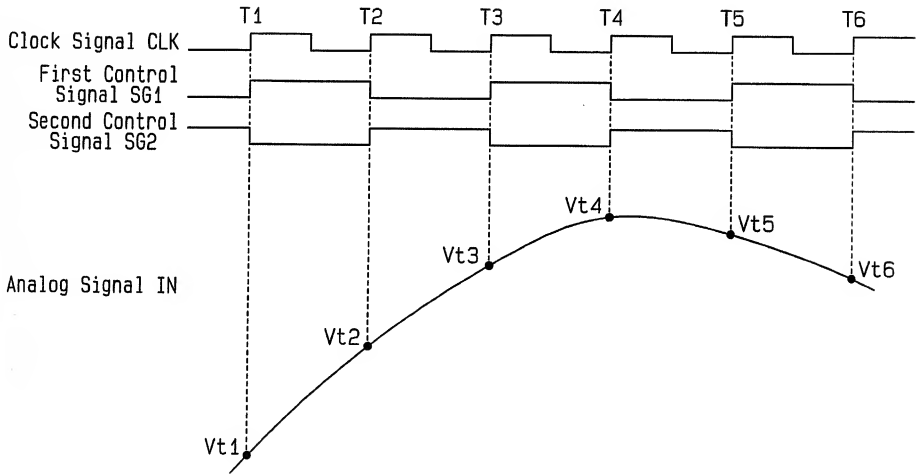


Fig.14

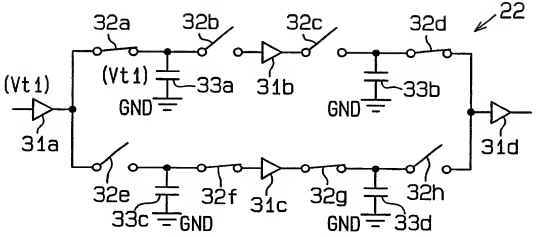


Fig.15

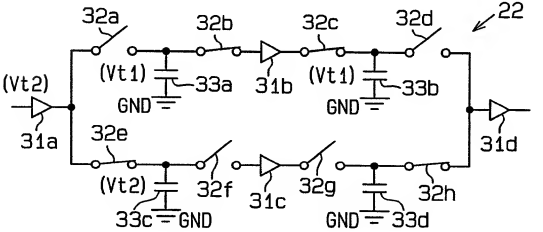


Fig.16

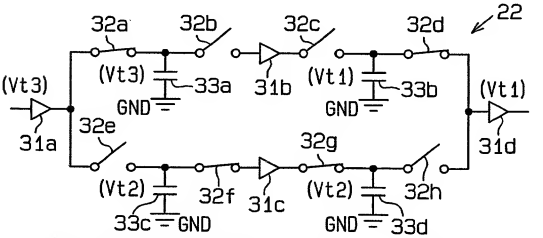


Fig.17

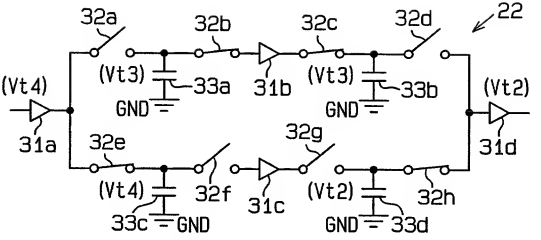


Fig.18

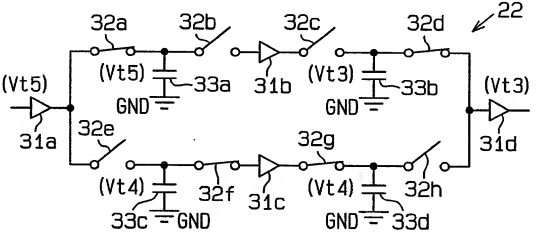


Fig.19

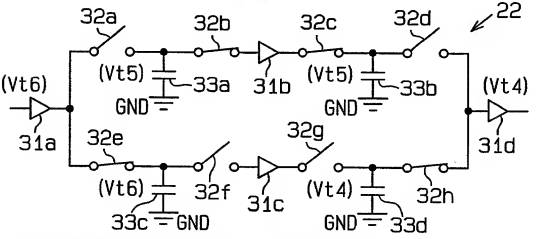


Fig.20

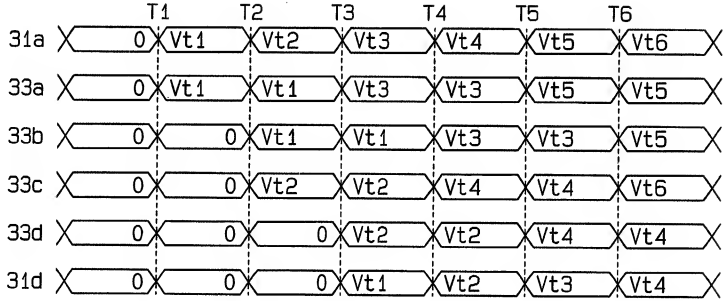


Fig.21

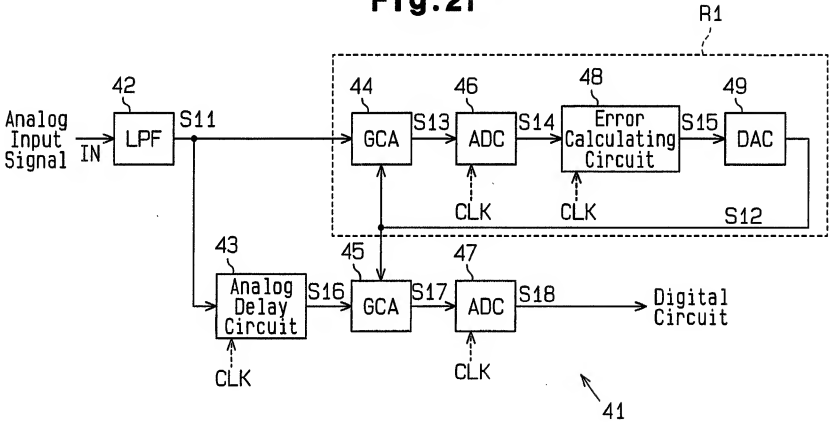


Fig.22

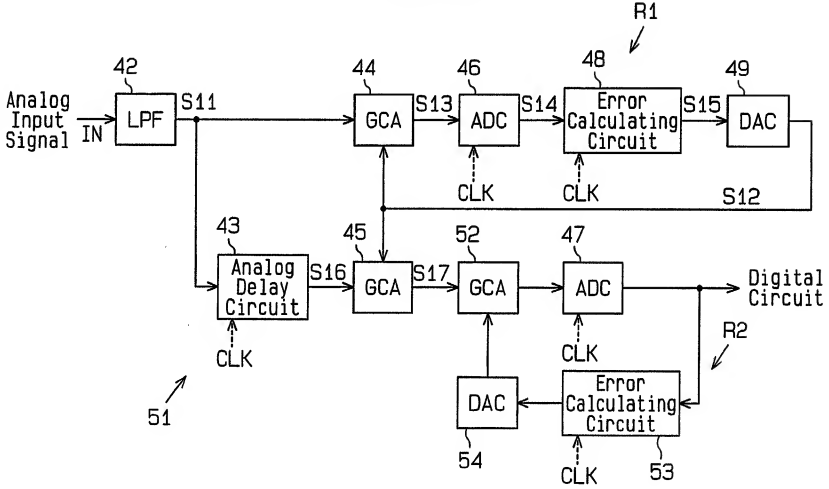


Fig.23

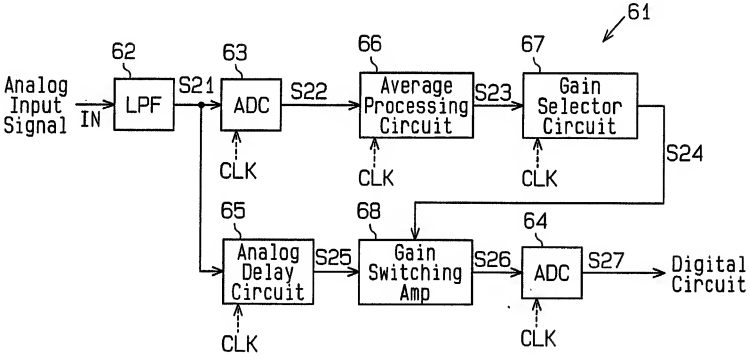


Fig.24

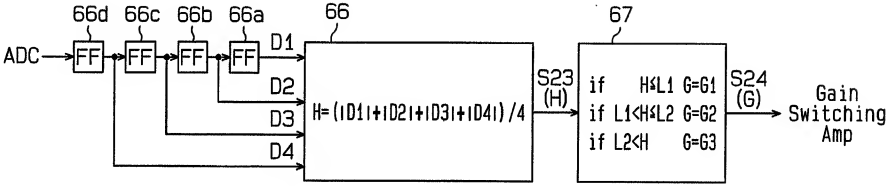


Fig.25

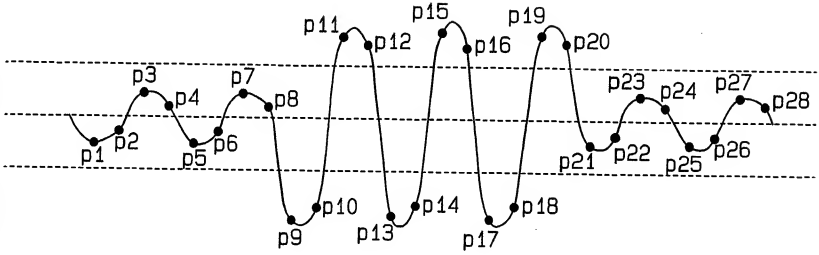

p1
p2
p3
p4
p5
p6
p7
p8
p9
p10
p11
p12
p13
p14
p15
p16
p17
p18
p19
p20
p21
p22
p23
p24
p25
p26
p27
p28

Fig.26

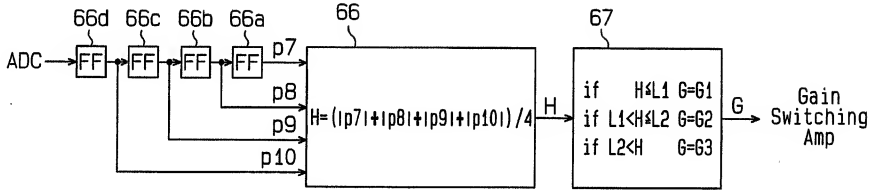


Fig.27

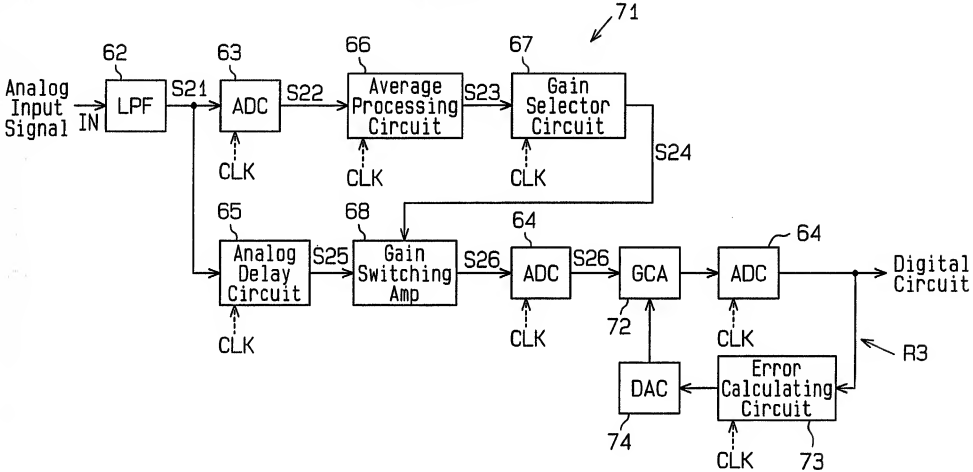


Fig.28

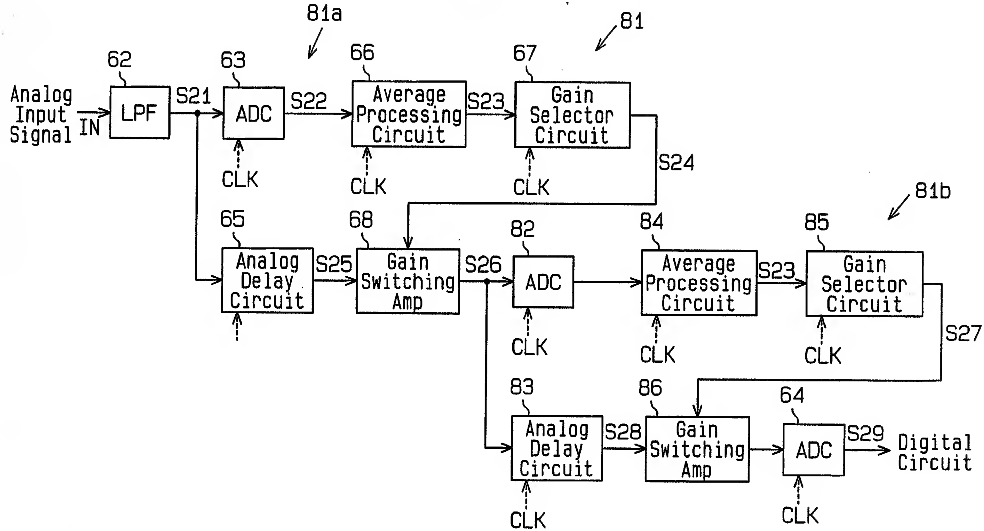
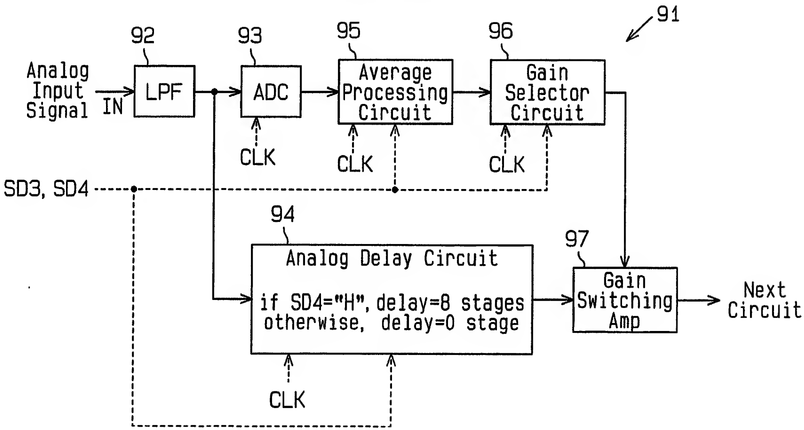

81a
81
81b
62
63
66
67
Analog Input Signal
IN
LPF
S21
ADC
S22
Average Processing Circuit
S23
Gain Selector Circuit
S24
CLK
65
68
82
84
85
Analog Delay Circuit
S25
Gain Switching Amp
S26
ADC
Average Processing Circuit
S23
Gain Selector Circuit
S27
83
86
64
Analog Delay Circuit
S28
Gain Switching Amp
ADC
S29
Digital Circuit

Fig.29



91
92
93
95
96
Analog Input Signal
IN
LPF
ADC
Average Processing Circuit
Gain Selector Circuit
CLK
CLK
CLK
SD3, SD4
94
97
Analog Delay Circuit
if SD4="H", delay=8 stages
otherwise, delay=0 stage
Gain Switching Amp
Next Circuit
CLK

Fig.30

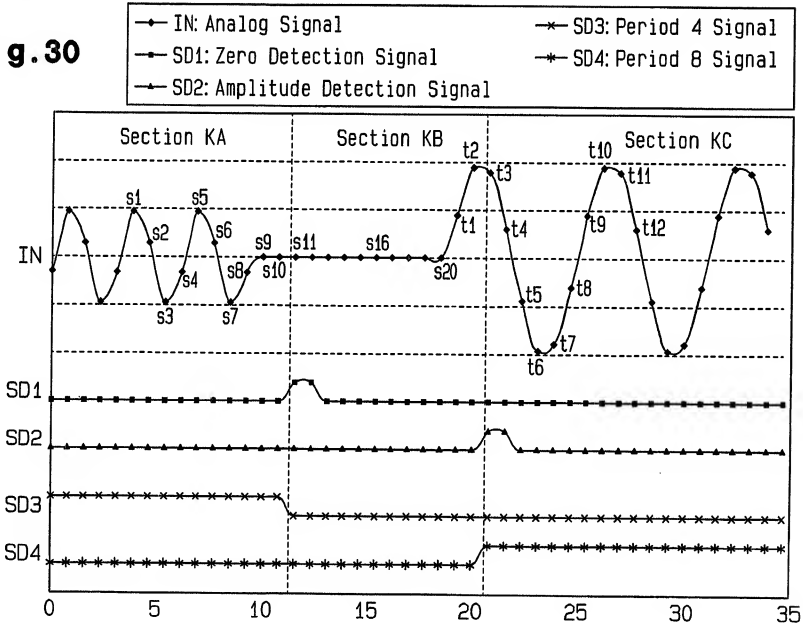


Fig.31

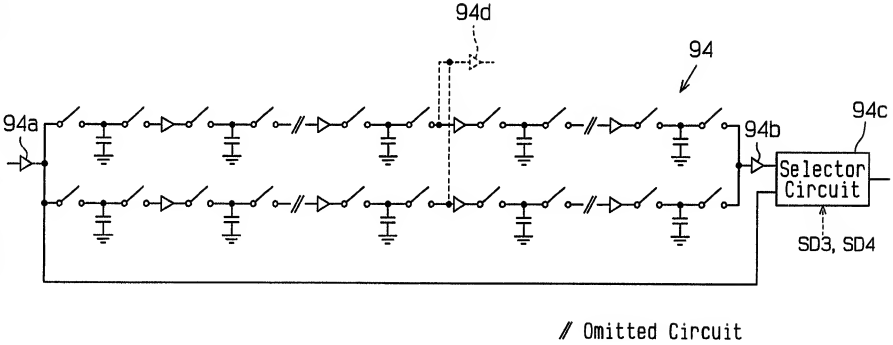


Fig.32

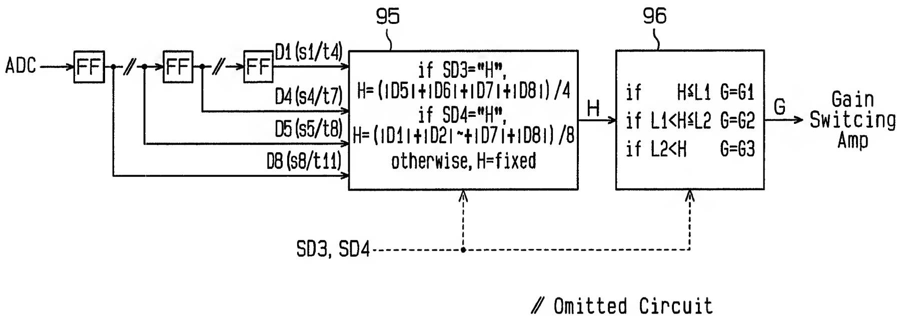

95
96
ADC
FF
FF
FF
D1 (s1/t4)
D4 (s4/t7)
D5 (s5/t8)
D8 (s8/t11)
if SD3="H",
H= (|D5|+|D6|+|D7|+|D8|) /4
if SD4="H",
H= (|D1|+|D2|~+|D7|+|D8|) /8
otherwise, H=fixed
H
if H≤L1 G=G1
if L1<H≤L2 G=G2
if L2<H G=G3
G
Gain Switcing Amp
SD3, SD4
// Omitted Circuit

Fig.33

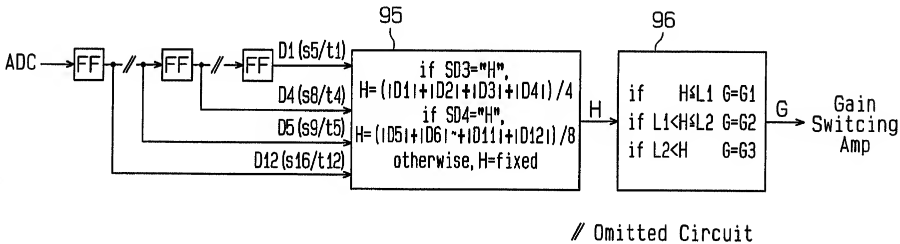

ADC
FF
FF
FF
D1 (s5/t1)
D4 (s8/t4)
D5 (s9/t5)
D12 (s16/t12)
95
if SD3="H",
H=(|D1|+|D2|+|D3|+|D4|)/4
if SD4="H",
H=(|D5|+|D6|~+|D11|+|D12|)/8
otherwise, H=fixed
H
96
if H≦L1 G=G1
if L1<H≦L2 G=G2
if L2<H G=G3
G
Gain Switcing Amp
// Omitted Circuit

Fig.34

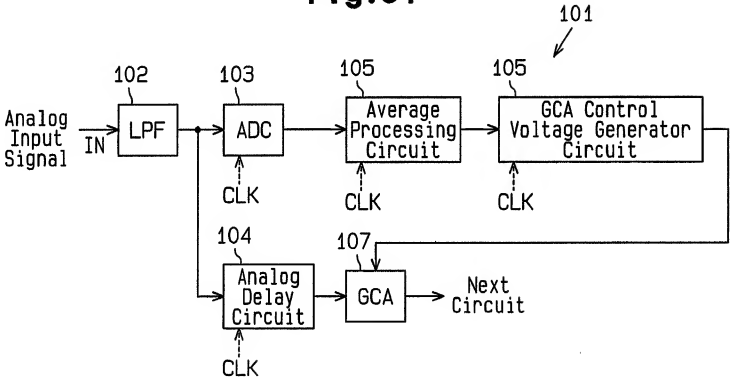


Fig.35